

## CLAIMS

1. A computer system, comprising:
  - a central processing unit (CPU);
  - a first bus coupled to the CPU;
  - a memory coupled to the first bus to store data accessible by the CPU via the first bus;
  - a second bus coupled to the first bus to provide communication with the CPU and the memory via the first bus; and
  - a PC card coupled to the second bus, the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system.
2. The computer system of claim 1 wherein the first bus comprises a local CPU bus and the second bus comprises a PCI bus.
3. The computer system of claim 2, further comprising a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device coupled to the PCI-CardBus bridge.
4. The computer system of claim 1 wherein the non-volatile memory of the PC card comprises a flash memory device.

5. The computer system of claim 1 wherein the PC card further includes a bus interface coupled to the second bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the second bus in accordance with a data format and transfer protocol of the second bus.

6. The computer system of claim 1, further comprising a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information.

7. The computer system of claim 1, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

8. The computer system of claim 1 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

9. A computer system, comprising:  
a central processing unit (CPU);  
a memory coupled to the CPU to store data accessible by the CPU;  
a bus coupled to the CPU and memory to provide communication therewith; and  
a PC card coupled to the bus, the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system.

10. The computer system of claim 9 wherein the bus comprises a PCI bus, and the computer system further comprises a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device coupled to the PCI-CardBus bridge.

11. The computer system of claim 9 wherein the non-volatile memory of the PC card comprises a flash memory device.

12. The computer system of claim 9 wherein the PC card further includes a bus interface coupled to the bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the bus in accordance with a data format and transfer protocol of the bus.

13. The computer system of claim 9, further comprising a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information.

14. The computer system of claim 9, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

15. The computer system of claim 9 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

16. An apparatus for capturing and restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory via a first bus, and further having a second bus coupled to the first bus to provide communication with the CPU and the memory, the apparatus comprising:

a PC card coupled to the second bus, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and

a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system.

17. The apparatus of claim 16, further comprising a bus interface coupled to the second bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the second bus in accordance with a data format and transfer protocol of the second bus.

18. The apparatus of claim 17 wherein the second bus is a PCI bus and the bus interface is CardBus compatible.

19. The apparatus of claim 16 wherein the non-volatile memory comprises a flash memory.

20. The apparatus of claim 16 wherein the transfer component comprises:  
a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and

a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

21. The apparatus of claim 16, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

22. An apparatus for capturing and restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory, and further having a bus coupled to the CPU and memory to provide communication with the CPU and the memory, the apparatus comprising:

a PC card coupled to the bus, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and

a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system.

23. The apparatus of claim 22, further comprising a bus interface coupled to the bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the bus in accordance with a data format and transfer protocol of the bus.

24. The apparatus of claim 23 wherein the bus is a PCI bus and the bus interface is CardBus compatible.

25. The apparatus of claim 23 wherein the non-volatile memory comprises a flash memory.

26. The apparatus of claim 23 wherein the transfer component comprises:  
 a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and  
 a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

27. The apparatus of claim 23, further comprising compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively.

28. An CardBus compatible PC card for restoring a machine state of a computer system having a central processing unit (CPU) coupled to a memory via a CPU bus, and further having a PCI bus coupled to the CPU bus to provide communication with the CPU and the memory, the PC card comprising:

an interface coupled to the PCI bus for transferring data thereto and therefrom;  
 a non-volatile memory coupled to the interface for storing and providing machine state information corresponding to the machine state;  
 a controller coupled to the interface and non-volatile memory to control the storing of machine state information in the non-volatile memory and the retrieval of the machine state information from the non-volatile memory; and  
 a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system.

29. The PC card of claim 28 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

30. The PC card of claim 28 wherein the non-volatile memory comprises a flash memory device.

31. The PC card of claim 28 wherein the transfer component comprises:  
a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory; and  
a download component for directing the controller to transfer data from the non-volatile memory to the CPU and the memory.

32. The PC card of claim 28, further comprising compression and decompression components for compressing the machine state information to be stored in the non-volatile memory and decompressing the stored compressed machine state information to be downloaded, respectively.

33. A computer system, comprising:  
a central processing unit (CPU);  
a local CPU bus coupled to the CPU;  
a memory coupled the local CPU bus to store data accessible by the CPU via the local CPU bus;  
a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus;  
a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and a CardBus compatible device;

a CardBus compatible PC card coupled to PCI-CardBus bridge, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and

a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system.

34. The computer system of claim 33 wherein the non-volatile memory of the PC card comprises a flash memory device.

35. The computer system of claim 33 wherein the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the non-volatile memory and the controller to transfer data between the memory and the PCI bus in accordance with the PCI data format and transfer protocol.

36. The computer system of claim 33, further comprising compression and decompression components for compressing the machine state information to be stored in the non-volatile memory and decompressing the stored compressed machine state information to be downloaded, respectively.

37. The computer system of claim 33 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.



38. In a computer system having a central processing unit (CPU) coupled to a memory, and further having a bus coupled to the CPU and memory to provide communication therewith, a method for storing a machine state of the computer system, comprising:

capturing the machine state of the computer system;

transferring machine state information corresponding to the captured machine state from the computer system to a PC card having a non-volatile memory; and

storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system.

39. The method of claim 38 wherein capturing, transferring and storing the machine state information is in response to executing a power down procedure.

40. The method of claim 38 wherein capturing, transferring and storing the machine state information is in response to a user request.

41. The method of claim 38 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

42. The method of claim 38 wherein capturing the machine state of the computer system comprises:

capturing data present in the memory; and

capturing data present in registers of the CPU.

43. The method of claim 38 wherein transferring the machine state information to the PC card comprises transferring data from the CPU and the memory to the PC card in accordance with a CardBus protocol.

44. The method of claim 38, further comprising compressing the machine state information to be stored in the non-volatile memory.

45. A method for restoring a machine state to a computer system having a central processing unit (CPU) coupled to a memory, and further having a bus coupled to the CPU and memory to provide communication therewith, the method comprising:

identifying machine state information corresponding to the machine state to which the computer system is to be restored stored in a non-volatile memory included in a PC card;

transferring the machine state information from the non-volatile memory to the computer system; and

writing data of the machine state information to the memory and CPU in order to restore the computer system to the identified machine state.

46. The method of claim 45 wherein identifying, transferring and writing the machine state information is in response to executing a power up procedure.

47. The method of claim 45 wherein identifying, transferring and writing the machine state information is in response to user request.

48. The method of claim 45 wherein the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory.

49. The method of claim 45 wherein transferring the machine state information from the non-volatile memory comprises transferring data from PC card to the computer system in accordance with a CardBus protocol.

50. The method of claim 45 wherein the machine state information stored in the non-volatile memory is in a compressed data format, and the method further comprises decompressing the machine state information to be transferred to the computer system.

50. The method of claim 45 wherein the machine state information stored in the non-volatile memory is in a compressed data format, and the method further comprises decompressing the machine state information to be transferred to the computer system.